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EXAMINER	
CHEN, TSE W	

ART UNIT	PAPER NUMBER
2116	6

DATE MAILED: 08/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/918,130	BRUCKNER ET AL.	
	Examiner	Art Unit	
	Tse Chen	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-9 and 11-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *13-17* is/are allowed.

6)☒ Claim(s) *1-3,5-9,11,12 and 18-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment A dated May 24, 2004.

2. Claims 1-3, 5-9, 11-26, are presented for examination. Applicant has canceled claims 4 and 10.

Claim Objections

3. Claim 7 is objected to because of the following informalities: "power down other components of the computer system" should be "power down the power consuming components" to be consistent with the existent antecedent. Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-2, 5, 7-8, 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hussain et al., U.S. Patent 6172611, hereinafter Hussain, in view of Baron et al., U.S. Patent 6098174, hereinafter Baron.

6. In re claim 1, Hussain discloses a method comprising:

- Receiving an indication of a thermal event in a processor [CPU 130], the processor being part of a computer system [100] [fig.1; col.4, ll.11-17; col.5, ll.13-19].
- In response to the indication of the thermal event, controlling a signal [ACPI related signal] [col.5, ll.42-53; ALERT# and related command issued is associated with ACPI

guidelines] and powering down the processor independently from the signal [col.5, ll.13-26; CPU powered down via Vcc coupling 172].

- Powering down other components of the computer system in response to the signal [col.5, ll.13-65; system is shut down with signal other than Vcc coupling 172; suggests ACPI related signal may be used to control power mode of other components].

7. Hussain did not discuss the details of the signal.

8. Baron discloses a method comprising:

- Controlling a signal [ACPI related pulse output] associated with a mechanical power switch [205] [col.7, ll.1-8; pulse output and related command issued is associated with ACPI guidelines].[1]
- Powering down other components of a computer system [100] in response to the signal [col.7, ll.1-8].

9. It would have been obvious to one of ordinary skill in the art, having the teachings of Hussain and Barron before him at the time the invention was made, to use the signal associated with a mechanical power switch as taught by Baron as the signal associated with a mechanical power switch taught by Baron is a known signal suitable for use with the system of Hussain. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to implement ACPI for critical state thermal management [Hussain: col.1, ll.37-56].

10. As to claim 2, Baron discloses said other components are located on a motherboard of the computer system [col.2, ll.25-28].

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[1] Note that ACDI [col.7, l.8] is a misprint. ACDI is better known as Asynchronous Communication Device Interface developed by IBM, instead of Intel. Intel's ACPI is better suited in the cited context in relation to power state management.

11. As to claim 5, Hussain discloses said powering down the processor comprises cutting off a supply voltage to the processor [col.5, ll.20-22].

12. In re claim 7, Hussain discloses a computer system [100] comprising:

- A processor [130] capable of indicating a thermal event [col.4, ll.7-17].
- A power supply subsystem [170] to supply power to the processor [fig.1].
- A circuit [thermal management IC 140] to:
    - In response to the indication of thermal event, control a signal [ACPI related signal] [col.5, ll.42-53; ALERT# and related command issued is associated with ACPI guidelines] and power down the processor independently from the signal [col.5, ll.13-26; CPU powered down via Vcc coupling 172].
    - Power down the power consuming components of the computer system in response to the signal [col.5, ll.13-65; system is shut down with signal other than Vcc coupling 172; suggests ACPI related signal may be used to control power mode of other components].

13. Hussain did not discuss the details of the signal.

14. Baron discloses a computer system [100] comprising:

- A processor [101].
- A mechanical switch [205], the switch being associated with a signal [pulse output which is also related to PSWITCHW].
- Power consuming components [fig.1; memory 102, etc.].
- A power supply subsystem [119] to supply power to the processor and power consuming components [fig.1].

- A circuit [fig.4; transistor 403] to:
    - Controlling a signal [ACPI related pulse output associated with the mechanical switch] [col.7, ll.1-8; pulse output and related command issued is associated with ACPI guidelines].[1]
    - Powering down the power consuming components of the computer system [100] in response to the signal [col.7, ll.1-8].

15. It would have been obvious to one of ordinary skill in the art, having the teachings of Hussain and Barron before him at the time the invention was made, to use the signal associated with a mechanical power switch as taught by Baron as the signal associated with a mechanical power switch taught by Baron is a known signal suitable for use with the system of Hussain. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to implement ACPI for critical state thermal management [Hussain: col.1, ll.37-56].

16. As to claim 8, Baron discloses said power consuming components are located on a motherboard of the computer system [col.2, ll.25-28].

17. As to claim 11, Hussain discloses the power supply subsystem that powers down the processor by cutting off a supply voltage to the processor [col.5, ll.20-22].

18. Claims 3, 6, 9, 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hussain and Baron as applied to claim 1 above, and further in view of Ceccherelli et at., U.S. Patent 5763960, hereinafter Ceccherelli.

19. In re claims 3, 6, 9, 12, Hussain and Baron disclose each and every limitation of the claim as discussed above in reference to claims 1 and 7. Hussain and Baron did not discuss the details of the powering down of the components.

20. As to claim 3, Ceccherelli discloses a method for powering down a computer system [fig.4], the method comprising introducing a predetermined delay after a receiving [activation] before a powering down other components of the computer [col.1, ll.28-30, col.10, ll.8-19].

21. As to claim 6, Ceccherelli discloses said powering down other components comprises cutting off at least one supply voltage to said other components [col.11, ll.63-67; col.12, ll.10-12].

22. As to claim 9, Ceccherelli discloses the computer system that introduces a delay in power down said power consuming components [col.1, ll.28-30, col.10, ll.8-19].

23. As to claim 12, Ceccherelli discloses the power supply subsystem that powers down the power consuming components by cutting off at least one supply voltage to said other components [col.11, ll.63-67; col.12, ll.10-12].

24. It would have been obvious to one of ordinary skill in the art, having the teachings of Hussain, Baron and Ceccherelli before him at the time the invention was made, to modify the system taught by Hussain and Baron to include the powering down of other components as taught by Ceccherelli, in order to obtain the system capable of sequentially powering down other components. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to efficiently power down a computer system in a controlled sequence [Ceccherelli: col.2, ll.22-41].

25. Claims 18, 21, 23, 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hussain in view of Howard et al., U.S. Patent 6711691, hereinafter Howard.

26. In re claim 18, Hussain discloses a method comprising:

- Receiving an indication of a thermal event in a processor [CPU 130], the processor being part of a computer system [100] [fig.1; col.4, ll.11-17; col.5, ll.13-19].
- In response to the indication of the thermal event, powering down the processor [col.5, ll.13-26; CPU powered down via Vcc coupling 172].

27. Hussain did not discuss a powering down sequence of other components relative to the processor in the computer system.

28. Howard discloses a method comprising:

- Powering down the processor [last processor] before powering down any other components of a computer system [100] [fig.1b; step 42 and then 44; col.6, ll.6-13].

29. It would have been obvious to one of ordinary skill in the art, having the teachings of Hussain and Howard before him at the time the invention was made, to modify the system taught by Hussain to include the powering down of other components as taught by Howard, in order to obtain the system capable of powering down the processor before powering down any other components. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to efficiently power down a computer system in a controlled sequence [Howard: col.2, l.56 – col.3, l.4].

30. As to claim 21, Hussain discloses said powering down the processor comprises removing a supply voltage to the processor [col.5, ll.20-22].

31. In re claim 23, Hussain discloses a computer system [100] comprising:

- A processor [130] capable of indicating a thermal event [col.4, ll.7-17].
- A power supply subsystem [170] to supply power to the processor [fig.1].

- A circuit [thermal management IC 140] to interact with the power supply subsystem [fig.1] to, in response to the processor indicating the thermal event [col.4, ll.7-17], power down the processor [col.5, ll.13-26; CPU powered down via Vcc coupling 172].

32. Hussain did not discuss a powering down sequence of other components relative to the processor in the computer system.

33. Howard discloses a computer system [100] comprising:

- A circuit [power manager 110] to power down the processor [last processor] before powering down any other components of the computer system [fig.1b; step 42 and then 44; col.6, ll.6-13].

34. It would have been obvious to one of ordinary skill in the art, having the teachings of Hussain and Howard before him at the time the invention was made, to modify the system taught by Hussain to include the powering down of other components as taught by Howard, in order to obtain the system capable of powering down the processor before powering down any other components. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to efficiently power down a computer system in a controlled sequence [Howard: col.2, l.56 – col.3, l.4].

35. As to claim 25, Hussain discloses the power supply subsystem that powers down the processor by removing a supply voltage to the processor [col.5, ll.20-22].

36. Claims 19, 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hussain and Howard as applied to claim18 above, and further in view of Baron.

37. In re claim 19, Hussain and Howard disclose each and every limitation of the claim as discussed above in reference to claim 18. Hussain and Howard did not discuss the location of the components.

38. Baron discloses a method for powering down other components of a computer system [100] in response to a signal [col.7, ll.1-8], the method wherein:

- The other components are located on a motherboard of the computer system [col.2, ll.25-28].

39. It would have been obvious to one of ordinary skill in the art, having the teachings of Baron, Hussain and Howard before him at the time the invention was made, to use the motherboard with the other components as taught by Baron as the motherboard taught by Baron is a well known configuration suitable for use with the system of Hussain and Howard. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to locate components of different functionalities in one board [Baron: col.2, ll.25-28].

40. In re claim 26, Hussain and Howard disclose each and every limitation of the claim as discussed above in reference to claim 23.

41. In particular, Hussain discloses a computer system [100] comprising:

- A circuit [thermal management IC 140] to control a signal [ACPI related signal] [col.5, ll.42-53; ALERT# and related command issued is associated with ACPI guidelines] to power down any other components of the computer system [col.5, ll.13-65; system is shut down with signal other than Vcc coupling 172; suggests ACPI related signal may be used to control power mode of other components].

42. Hussain did not discuss the details of the signal.

43. Baron discloses a computer system [100] comprising:

- A processor [101].
- A mechanical switch [205] associated with a signal [pulse output which is also related to PSWITCHW] to power on and off the computer system [col.7, ll.1-8].
- Other components of the computer system [fig.1; memory 102, etc.].
- A circuit [fig.4; transistor 403] controls the signal [ACPI related pulse output associated with the mechanical switch] [col.7, ll.1-8; pulse output and related command issued is associated with ACPI guidelines][1] to power down any other of the computer system [col.7, ll.1-8].

44. It would have been obvious to one of ordinary skill in the art, having the teachings of Hussain, Howard and Barron before him at the time the invention was made, to use the signal associated with a mechanical power switch as taught by Baron as the signal associated with a mechanical power switch taught by Baron is a known signal suitable for use with the system of Hussain and Howard. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to implement ACPI for critical state thermal management [Hussain: col.1, ll.37-56].

45. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hussain and Howard as applied to claim 18 above, and further in view of Applicant's Admission of Prior Art.

46. Hussain and Howard disclose each and every limitation of the claim as discussed above in reference to claim 18. Hussain and Howard did not discuss how a computer system is conventionally powered down.

47. Applicant's Admission of Prior Art discloses the conventional method of powering down a computer system [background; pg.1, ll.11-15], the method comprising:

- Introducing a delay [pg.1, ll.11-14].
- Determining whether a mechanical power switch has been in an off position for the duration of the delay [pg.1, ll.12-15].

48. It would have been obvious to one of ordinary skill in the art to incorporate the teachings of Hussain and Howard with the conventional method of powering down a computer system disclosed by the Applicant, in order to obtain the system capable of powering down the processor before powering down any other components. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to efficiently power down a computer system in a controlled sequence [Howard: col.2, l.56 – col.3, l.4].

49. Claims 22, 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hussain and Howard as applied to claim 18 above, and further in view of Ceccherelli.

50. In re claims 22, 24, Hussain and Howard disclose each and every limitation of the claim as discussed above in reference to claim 18. Hussain and Howard did not discuss the details of the powering down of the components.

51. As to claim 22, Ceccherelli discloses the powering down any other components that comprises cutting off at least one supply voltage to said any other components of a computer system [col.11, ll.63-67; col.12, ll.10-12].

52. As to claim 24, Ceccherelli discloses the computer system that introduces a delay in powering down any other components of the computer system [col.1, ll.28-30, col.10, ll.8-19].

53. It would have been obvious to one of ordinary skill in the art, having the teachings of Hussain, Howard and Ceccherelli before him at the time the invention was made, to modify the system taught by Hussain and Howard to include the powering down of other components as taught by Ceccherelli, in order to obtain the system capable of sequentially powering down other components. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to efficiently power down a computer system in a controlled sequence [Ceccherelli: col.2, ll.22-41].

Allowable Subject Matter

54. Claims 13-17 are allowed.

55. The following is a statement of reasons for the indication of allowable subject matter: the claims are allowable because none of the reference, either alone or in combination discloses or renders obvious the method of claim 13 where "in response to the indication, introducing a delay, and determining whether a mechanical power switch has been in an off position for the duration of the delay."

Response to Arguments

56. Applicant's arguments, with respect to the Summary of the Invention in the Specification and claims 12 and 13, have been fully considered and are persuasive. The objections of the missing Summary of the Invention in the Specification and claims 12 and 13 have been withdrawn.

57. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

58. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Barlow et al., U.S. Patent 5367697, discloses powering down a processor before any other components.

b. Peters et al., U.S. Patent 5379378, discloses powering down a computer system with a signal.

59. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (703) 305-8580. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (703) 308-1159. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tse Chen
July 26, 2004

REHANA PERVEEN
PRIMARY EXAMINER